CLOCK AND DATA RECOVERY CIRCUIT WITHOUT JITTER PEAKING

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BACKGROUND OF THE INVENTION

5   ### Field of the Invention

This invention relates to clock recovery circuits and more particularly to phase locked loops used to recover a clock and data from an input data stream.

Description of the Related Art

It is common to transmit data streams with an implied clock. When the data

10   stream is decoded, the clock is extracted from the data and regenerated. The data is then resynchronized to the extracted clock. Traditionally, a phase locked loop (PLL) has been used to perform the clock recovery operation. Fig. 1A shows a block diagram of a traditional PLL configured for a clock and data recovery application. The phase locked loop 100 includes a phase detector 102, which receives the input

15   data signal conveyed on node 104 and also receives the output clock signal conveyed on node 106 from the voltage controlled oscillator (VCO) 108. The phase detector 102 generates an error signal 110, which is a function of the phase difference between the input data signal and the VCO output clock signal. The phase detector 102 may also include additional circuitry to generate the reconstructed data on output node

20   114.

The loop amplifier and filter block 112 typically includes a gain block 120, an integrator block 122, and a summer block 124, shown in Fig. 1B. The loop amplifier and filter block 112 low-pass filters the output of the phase detector 102 to generate a control signal on node 116 that is provided to the VCO 108. VCO 108 adjusts the

25   output clock signal on node 106 in response to the control signal to track the input data signal.

- 1 -

In data/clock recovery systems, traditional PLLs have two significant drawbacks. First, the stabilizing zero in the loop gain equation produces jitter peaking in the closed loop transfer response. In order to appreciate this issue, a brief description of the frequency response of the traditional PLL is set forth. Fig. 1C,

5   illustrates the linear block diagram of the PLL shown in Fig. 1A. Equation 1 sets forth the closed loop transfer function, G(s), of traditional PLL 100 , where τ_1 is the time constant of the explicit zero and K_1 is the combined gain of the loop amplifier and filter, the phase detector and the VCO.

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$$G(s) = \frac{K_1(1 + \tau_1 s)}{s^2 + K_1 \tau_1 s + K_1} \qquad \text{(Eq. 1)}$$

Fig. 2 shows a graph of the frequency response of the closed loop transfer function. As can be seen in the graph, the magnitude of the transfer function is fairly constant at low frequency, and increases slightly for a band of frequencies labeled 200, where the transfer function exceeds unity and results in jitter peaking.

15   The magnitude of that peaking is very critical for many applications. For example, the Synchronous Optical Network (SONET) standard limits the acceptable peaking to 0.1 dB. If allowed to exceed this limit, frequency components of input data jitter which fall within this peaking region are actually amplified by the PLL. If several such PLLs are coupled sequentially, the jitter may be amplified to a degree

20   which severely compromises the ability to meet jitter tolerances, or even to correctly recover data.

A second problem characteristic of traditional PLLs is that the jitter tolerance and the jitter transfer characteristic are both tied to the same circuit parameter (gain K_1) and cannot be independently optimized.

25   A solution to the two problems described above was proposed in U.S. Pat. No. 5,036,298 to Bulzachelli. Unlike the traditional PLL system shown in Fig. 1, the system shown in Fig. 3 delays the incoming data on node 303 by an amount determined by the control voltage on node 305. Note that the incoming data is regenerated by additional logic in phase detector 309 and is retimed to be

30   synchronous with the output clock from VCO 311 on node 312. It is desirable for the system shown in Fig. 3 that the delay provided be a well controlled delay with respect

- 2 -

to voltage, independent of the input data pattern. That can be difficult for high speed applications whose circuits do not completely reach a static condition between input transitions.

5   Therefore, it would be desirable to solve the jitter peaking problem for high speed applications while avoiding the data pattern dependencies associated with prior art PLL structures.

SUMMARY OF THE INVENTION

Accordingly, the invention provides a delay circuit that operates on the VCO output clock instead of the input data, thereby eliminating any delay versus input data
10   pattern issue.

In one embodiment a clock recovery circuit is provides that includes a phase detector circuit that generates a difference signal indicating a phase difference between an incoming data stream and a delayed clock signal. A loop filter circuit receives the difference signal and supplies a filtered output as a control signal to an
15   oscillator circuit as in a conventional PLL circuit. The oscillator circuit responds to the control signal to generate an output clock signal that varies according to the control signal to track the input data signal. A delay clock circuit receives a delay control signal derived from the difference signal and outputs the output clock signal delayed according to the delay control signal, as the delayed clock signal. In one
20   embodiment the delay control signal is the same control signal supplied to the VCO.

In another embodiment, a method is provided for recovering a clock signal from an incoming data stream. The method includes determining a phase difference between an input data stream and a delayed clock signal in a phase detector and generating a difference signal indicative thereof. A control signal is generated from
25   the difference signal to control an oscillator, which generates an output clock that varies according to the control signal. A delayed version of the output clock is created in a delay circuit with the delay being dependent upon a delay control signal derived from the difference signal. That delayed version is supplied to the phase detector as the delayed clock signal.

- 3 -

In order to provide recovered data that is retimed to the output clock rather than the delayed clock, a FIFO memory may be used in which the delayed clock signal is used as the FIFO write clock and the output clock is used as the FIFO read clock. Alternatively, a series of successively coupled registers clocked by

5   intermediate signals from the delay clock circuit can be used to gradually shift the data from the delayed clock to the output clock.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the

10   accompanying drawings.

Fig. 1A depicts a prior art clock and data recovery circuit.

Fig. 1B depicts additional details on the loop filter shown in Fig. 1A.

Fig. 1C shows a linear block diagram for the traditional clock and data recovery circuit shown in Fig 1A.

15   Fig. 2 is a graph of the frequency response of this closed loop transfer function G(s) of the traditional PLL circuit shown in Fig. 1A.

Fig. 3 depicts a prior art clock and data recovery circuit that overcomes the jitter peaking problem found in the PLL system shown in Fig. 1A.

Fig. 4A depicts an embodiment of a clock recovery circuit according to the

20   present invention.

Fig. 4B depicts a linear block diagram for the clock recovery circuit illustrated in Fig 4A.

Fig. 5 depicts another embodiment of a clock recovery circuit according to the present invention.

25   Fig. 6 depicts one embodiment for retiming input data according to the present invention.

- 4 -

Fig. 7 depicts another embodiment for retiming input data according to the present invention.

The use of the same reference symbols in different drawings indicates similar or identical items.

5   **DESCRIPTION OF THE PREFERRED EMBODIMENT(S)**

Referring to Fig. 4A, a block diagram of a phase locked loop (PLL) configured for a clock and data recovery application according to the present invention is shown. Rather than delaying the data, the phase locked loop 400 delays the feedback clock supplied to phase detector 402. More specifically, phase detector

10   402 receives the input data signal conveyed on node 404 and the delayed clock signal conveyed on node 406 from the voltage controlled delay circuit 408. Voltage controlled delay circuit 408 receives the output clock on node 410 from voltage controlled oscillator (VCO) 412. The phase detector 402 generates an error signal on node 414, which is a function of the phase difference between the input data signal

15   and the delayed clock signal. The loop filter 416 functions conventionally as a low pass filter for the error signal 414 and generates the control signal on node 418, which causes VCO 412 to adjust the output clock on node 410 to track the input data signal. The control signal 418 is used both to adjust the phase of the VCO output clock on node 410 as well as control the amount that the output clock is delayed in delay circuit

20   408.

The phase detector 402 may also include additional circuitry known in the art to generate the reconstructed data on output node 420 that is retimed to the delay clock. Alternatively, the additional circuitry may be outside the phase detector. In a typical implementation, once the clock input to the phase detector (signal 406) and the

25   input data are properly aligned by the phase detector, the clock 406 is used to strobe the input data into a flip-flop, thus generating retimed data synchronized to the delayed clock signal 406.

Referring to Fig. 4B a linearized block diagram illustrates the transfer function associated with the PLL shown in Fig. 4A. The blocks in Fig. 4B have the same

reference numbers as the blocks shown in Fig. 4A to indicate that their correspondence. From Fig. 4B, it can be shown that:

$$\phi_{VCO} = \frac{K_2}{s} V_1$$ (Eq. 2)

$$V_1 = \frac{1}{s} \left[\phi_{DATA} - (\phi_{VCO} + K_2 \tau_2 V_1) \right]$$ (Eq. 3)

5   The closed loop transfer function G(s) is:

$$G(s) = \frac{\phi_{VCO}}{\phi_{DATA}} = \frac{K_2}{s^2 + K_2 \tau_2 s + K_2}$$ (Eq. 4)

In the above equation K_2 represents the VCO gain in MHz/V and $K_2 \tau_2$ is defined as the phase shift in the delay line per volt at V_1 (in units of S/V).

Delaying the clock allows the zero in the closed loop response to be
10   eliminated and thus eliminates the jitter peaking problem illustrated in Fig. 2. Further, because the delay is accomplished by delaying the clock rather than the data, the delay is data pattern independent.

Another embodiment of the invention is illustrated in Fig. 5. Rather than use the same filter to generate the control voltage for VCO 412 and clock delay circuit
15   408, a separate filter 422 is used to generate the delay control signal on node 424.

Referring Figs. 4 and 5, note that the retimed data provided on node 420 is retimed to the delay clock supplied on node 406 (since that is the only clock received in that block), rather that the output clock from VCO 412. However, the data should be retimed to the output clock from the VCO. Various approaches described further
20   herein can be used to accomplish that task.

Fig. 6 shows one embodiment to retime the recovered data from the delayed clock to the VCO output clock. Assume the data is recovered in a conventional manner using the delayed clock 406, as described previously. The data, synchronized to the delay clock, is provided on node 420 to first in first out (FIFO) buffers 603.
25   The data is written into the FIFO with the delayed clock supplied from node 406. The

- 6 -

VCO output clock on node 410 is supplied to the FIFO as the read clock and the data is read out on node 607. Thus, in order to retime the data, the data is written into the FIFO using the delayed clock as the FIFO write clock and read out of the FIFO using the VCO output clock as the FIFO read clock.

5   Fig. 7 illustrates another embodiment for retiming the data from the delayed clock to the VCO output clock. An exemplary voltage controlled delay circuit 408 includes a plurality of stages 701, 703 and 705. Loop filter 416 (see Fig. 4) supplies the voltage control signal on node 418 to control the propagation of the VCO output clock through the delay circuit 408. As described previously, phase detector 402 receives the delay clock supplied on node 406. A plurality of registers 712, 714, and 716 are successively coupled and clocked by respective intermediate outputs from the voltage controlled delay circuit 408. In particular, the phase detector 402 supplies the data retimed to the delayed clock on node 420 to register 712, which is clocked by intermediate output signal 713. Register 714, which receives data from register 712, is clocked by intermediate delay clock output 715. Data is moved successively in each register stage to a less delayed clock that is closer to the actual VCO output clock. Finally, register 716 is clocked by the VCO output clock supplied on node 410. The data in register 716 is thus synchronized to the VCO output clock rather than the delayed clock. Note that the number of delay stages and the number of registers used is exemplary only. The delay from one stage to the next should be less than one period of the output clock.

The need to retime the data to the VCO output clock rather than the delayed clock adds some complexity over the prior art where the data is provided retimed to the VCO output clock initially. Note, however, that the added complexity is in digital logic in an architecture that eliminates an analog problem that can result in increased output clock jitter.

The description of the invention set forth herein is illustrative, and is not intended to limit the scope of the invention as set forth in the following claims. For example, while the oscillator and the delay circuit have been described as voltage controlled, current controlled circuits could also be used. In addition a variety of storage elements (e.g., latches, flip-flops, etc.) could be used for FIFO 603 and registers 712-716. Other variations and modifications of the embodiments disclosed

- 7 -

herein, may be made based on the description set forth herein, without departing from the scope and spirit of the invention as set forth in the following claims.

- 8 -